CLAIMS

What is Claimed is:

1. A current limiting circuit voltage regulation comprising:

a device coupled to an output node of the current limiting circuit, said device responsive to magnitude of a signal at said output node, wherein said device has a first mode and a second mode depending on the magnitude of the signal;

a regulation component coupled to the device that regulates a voltage at said output node when said device is in said first mode; and

an element coupled to the device that limits current at said output node when said device is in said second mode.

2. The circuit of Claim 1, wherein the element that limits current at said output node when said device is in said second mode clamps a voltage at a control gate of an output transistor to limit said current at said output node.

3. The circuit of Claim 1, wherein the element that limits current at said output node when said device is in said second mode has a current that is mirrored in an output transistor to limit said current at said output node.

4. The circuit of Claim 1, wherein said device is in a feedback loop comprising said regulation component and wherein said feedback loop is broken when said device is in said second mode.

5. The circuit of Claim 1, wherein the device acts as a buffer between said regulation component and said output in said first mode.

6. The circuit of Claim 1, wherein the device effectively operates as a resistive switch in said second mode.

7. The circuit of Claim 1, wherein the device is controlled between said first mode and said second mode by the output of said regulation component.

8. A current limiting voltage regulation circuit comprising:

an output transistor having a control terminal;

an error amplifier having a first input coupled to said output transistor and a second input that can receive a reference voltage;

a first transistor coupled between said control terminal of said output transistor and an output of said error amplifier, said first transistor responsive to magnitude of a signal at said output transistor, wherein said first transistor has a first mode and a second mode depending on the magnitude of the signal, wherein said error amplifier regulates a voltage of

said output transistor based on said reference voltage if said first transistor is in said first mode; and

a second transistor coupled to said first transistor and said output transistor, wherein a current through said second transistor is mirrored in said output transistor if said first transistor is in said second mode.

9. The circuit of Claim 8, wherein said first transistor is in a feedback loop comprising said error amplifier and wherein said feedback loop is broken when said first transistor is in said second mode.

10. The circuit of Claim 8, wherein said second transistor clamps a voltage at a control gate of said output transistor if said first transistor is in said second mode.

11. The circuit of Claim 8, wherein a drain of said first transistor is clamped at a pre-determined voltage.

12. The circuit of Claim 8, wherein said first transistor operates in a triode region in said second mode allowing said second transistor to function as a current mirror with said output transistor.

13. The circuit of Claim 8, further comprising a current source feeding said first transistor and a current sink draining said first transistor,

wherein substantially the difference between the current sink and source flow through said second transistor.

14. The circuit of Claim 8, further comprising a cascode transistor coupled to said output transistor.

15. The circuit of Claim 8, wherein said current limiting circuit is a low dropout (LDO) regulation circuit.

16. The circuit of Claim 8, wherein said first transistor and said second transistor are coupled by their respective drains.

17. A method of controlling current and regulating voltage, comprising:

a) sensing a signal at an output node;

b) if said signal is below a pre-determined threshold, regulating a voltage at said output node; and

c) if said signal is above said pre-determined threshold, limiting a current at said output node without regulating said voltage at said output node.

18. The method of Claim 17, wherein said c) comprises limiting a voltage at a control gate of an output transistor to a predetermined level to limit said current at said output node.

19. The method of Claim 17, wherein said c) comprises mirroring a current in a regulation loop to said output node.

20. The method of Claim 17, wherein said c) comprises preventing a regulation component from regulating said voltage at said output node.